DETAILED ACTION

1. Claims 1-12 are pending and have been examined.

2. Claims 1-12 are rejected.

Response to Arguments

3. Applicant's arguments, see pages 5-6 of the remarks, filed March 14, 2008, with respect to the rejection(s) of claim(s) 1-12 under 35 U.S.C. § 102(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn, in light of the amendments to the independent claims. However, upon further consideration, a new ground(s) of rejection is made in view of US Patent No. 6,912,651 (hereinafter Hamdi). Hamdi teaches (Fig. 6) a computer system having USB Host Controller **608** that is directly connected to a system/memory bus **604** which directly interfaces system memory **606** and processor **602** (col. 11, ll. 42-64). By directly interconnecting the USB Host Controller, system memory and processor via a common bus, the USB Host Controller access the system memory directly and is not burdened with additional latency associated with having to access the system memory through a processor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2002/0116565 (hereinafter Wang) in view of US Patent No. 6,912,651 (hereinafter Hamdi).

As previously discussed in the Final Office Action dated January 18, 2008, Wang discloses: a host controller (Fig. 1A, 100), for use in a bus communication device comprising a host microprocessor and a system memory, the host controller comprising: a first interface (Fig. 1A, the left side of host controller 100) for connection to a memory bus (Fig. 1A, 31) which connects the host microprocessor (Fig. 1A, 24) and the system memory (Fig. 1A, 32), such that the host controller is adapted to act only as a slave on the memory bus ([0138-0140] describe how the host controller is not required to act as a bus master); an internal memory (Fig. 1A, 30), for storing a plurality of transfer-based transfer descriptors received through the first interface ([0041]); and a second interface (Fig. 1A, 28 the right side of host controller), for connection to an external bus (Fig. 1A, the lines connecting to USB devices 26), wherein the host controller is adapted to: execute stored transfer-based transfer descriptors ([0041-0042]); update the content of the stored transfer-based transfer descriptors on execution ([0051] "...and updates, in state 76, a record in the transaction descriptor..."); and copy the updated stored transfer-based transfer descriptors to the system memory ([0138-0140] describes the processes of where the host controller transfers data to the system memory under the control of the microprocessor). While the host controller provides a connection to system memory and a microprocessor, Wang does not expressly disclose providing a direct connection to both system memory and the microprocessor.

Hamdi teaches (Fig. 6) a computer system having USB Host Controller **608** that is directly connected to a system/memory bus **604** which directly interfaces system memory **606** and processor **602** (col. 11, ll. 42-64). By directly interconnecting the USB Host Controller, system memory and processor via a common bus, the USB Host Controller access the system memory directly and is not burdened with additional latency associated with having to access the system memory through a processor.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to directly connect the USB Host Controller of Wang to the system memory and microprocessor as suggested by Hamdi such that memory access latency is reduced because the USB Host Controller does not need to access the system memory through the microprocessor.

For claim 1 Wang in view of Hamdi teach:
A host controller (Fig. 1A, 100), for use in a bus communication device comprising a host microprocessor and a system memory, the host controller comprising:

- a first interface (Fig. 1A, the left side of host controller 100) for direct connection (Hamdi teaches, Fig. 6, providing a direct connection between the host controller, microprocessor and system memory [col. 11, ll. 42-64].) to a memory bus (Fig. 1A, 31) which connects the host microprocessor (Fig. 1A, 24) and the system memory (Fig. 1A, 32), such that the host controller is adapted to act only as a slave on the memory bus ([0138-0140] describe how the host controller is not required to act as a bus master);

- an internal memory (Fig. 1A, 30), for storing a plurality of transfer-based transfer descriptors received through the first interface ([0041]); and
- a second interface (Fig. 1A, 28 the right side of host controller), for connection to an external bus (Fig. 1A, the lines connecting to USB devices 26),
- wherein the host controller is adapted to:
    - execute stored transfer-based transfer descriptors ([0041-0042]);
    - update the content of the stored transfer-based transfer descriptors on execution ([0051] "…and updates, in state 76, a record in the transaction descriptor…"); and
    - copy the updated stored transfer-based transfer descriptors to the system memory ([0138-0140] describes the processes of where the host controller transfers data to the system memory under the control of the microprocessor).

For claim 2 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the internal memory is a dual-port RAM ([0054]).

For claim 3 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the internal memory is a single-port RAM, and the host controller further comprises an arbiter to allow data to be written to and read from the RAM essentially simultaneously ([0056] "The batch memory 30 is preferably organized as to be able to receive USB transactions from the host microprocessor 24 for one batch while the host controller system 100 is acting on another batch.").

For claim 4 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the internal memory is divided into two parts (Fig. 5, first part 106 and second part 116), and is adapted to store transfer-based transfer descriptor headers in a first part ([0060]), and to store transfer-based transfer descriptor payload data in a second part ([0063]).

For claim 5 Wang in view of Hamdi teach:

A host controller as claimed in claim 4, wherein the first part of the internal memory is sub-divided into two sub-parts, and is adapted to store transfer descriptor headers relating to periodic transfers in a first sub-part ([0062,0065] "isochronous transaction"), and to store transfer descriptor headers relating to asynchronous transfers in a second sub-part ([0065] "bulk transaction"]).

For claim 6 Wang in view of Hamdi teach:

A host controller as claimed in claim 5, wherein the host controller is adapted to scan the first sub-part of the internal memory once in each micro-frame ([0065] "For example, five transactions can be scheduled for a total of 1,280 bytes in one ms: one isochronous of 1023 and four bulk or interrupt transactions of 64 bytes each." The host controller therefore scanned the control memory [CM] once in the micro-frame thus meeting the claim limitation.), and is adapted to scan the second sub-part continuously throughout each micro-frame ([0065] "For example, five transactions can be scheduled for a total of 1,280 bytes in one ms: one isochronous

of 1023 and four bulk or interrupt transactions of 64 bytes each." The host controller therefore scanned the control memory [CM] throughout the micro-frame thus meeting the claim limitation.).

For claims 7 and 11 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the host controller is a USB host controller and the second interface is a USB bus interface (Fig. 1A, [0003, 0016]).

For claims 8 and 12 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the internal memory is adapted to store multiple micro-frames of transfer descriptors ([0056] "The batch memory 30 is preferably organized so as to be able to receive USB transactions from the host microprocessor 24 for one batch while the host controller system 100 is acting on another batch."), and to execute the stored transfer descriptors without intervention from the host microprocessor ([0042] describes how the host controller executes the stored transfer descriptors without the microprocessor.).

For claim 9 Wang in view of Hamdi teach:

A host controller as claimed in claim 8, wherein each of the multiple micro-frames of transfer descriptors may store payload data relating to one or more of isochronous, interrupt and bulk data transfers ([0063, 0070] describe a data memory 116 [Fig. 5] holds data for USB transactions of type isochronous, bulk or interrupt [0062,0065].).

For claim 10 Wang in view of Hamdi teach:

A bus communication device, comprising:

- a host microprocessor (Fig. 1A, 24);
- a system memory (Fig. 1A, 32);
- a memory bus, which connects the host microprocessor and the system memory (Fig. 1A line connecting 24 and 32; and
- a host controller (Fig. 1A, 100), wherein the host microprocessor is adapted to form transfer-based transfer descriptors, and write the transfer-based transfer descriptors to the system memory and to the host controller, and wherein the host controller comprises:
    - a first interface (Fig. 1A, the left side of host controller 100) for direct connection (Hamdi teaches, Fig. 6, providing a direct connection between the host controller, microprocessor and system memory [col. 11, ll. 42-64].) to a memory bus (Fig. 1A, 31) which connects the host microprocessor (Fig. 1A, 24) and the system memory (Fig. 1A, 32), such that the host controller is adapted to act only as a slave on the memory bus ([0138-0140] describe how the host controller is not required to act as a bus master);
    - an internal memory (Fig. 1A, 30), for storing a plurality of transfer-based transfer descriptors received through the first interface ([0041]); and
    - a second interface (Fig. 1A, 28 the right side of host controller), for connection to an external bus (Fig. 1A, the lines connecting to USB devices 26),
    - wherein the host controller is adapted to:
        - execute stored transfer-based transfer descriptors ([0041-0042]);

- update the content of the stored transfer-based transfer descriptors on execution ([0051] "...and updates, in state 76, a record in the transaction descriptor..."); and
- copy the updated stored transfer-based transfer descriptors to the system memory ([0138-0140] describes the processes of where the host controller transfers data to the system memory under the control of the microprocessor).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN M. STIGLIC whose telephone number is (571)272-3641. The examiner can normally be reached on Monday - Friday (7:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571.272.3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R. M. S./
Examiner, Art Unit 2111

/Paul R. Myers/
Primary Examiner, Art Unit 2111